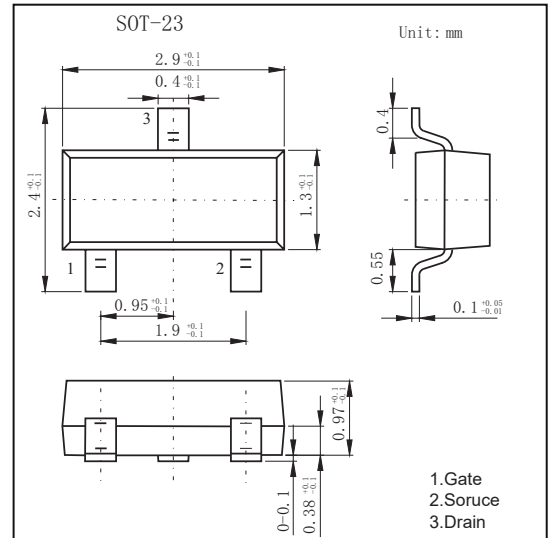


**SOT-23 Plastic-Encapsulate MOSFETS**
**FEATURE**

- High dense cell design for extremely low RDS(on) @VGS=4.5V
- 5V Logic Level Control
- Exceptional on-resistance and maximum DC current capability
- N-Channel Enhancement Mode Field Effect Transistor

**MECHANICAL DATA**

- Case style:SOT-23molded plastic
- Mounting position:any


**MAXIMUM RATINGS AND CHARACTERISTICS**

@ 25°C Ambient Temperature (unless otherwise noted)

Parameter	Symbol	Rating	Unit	
Gate-Source Voltage	$V_{GS}$	±12	V	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	30	V	
Maximum Junction Temperature	$T_J$	150	°C	
Storage Temperature Range	$T_{STG}$	-50 to 150	°C	
Pulse Drain Current Tested①	$I_{DM}$	23	A	
Continuous Drain Current( $V_{GS}=4.5V$ )	$I_D$	$T_A=25^\circ C$	5.8	A
		$T_A=70^\circ C$	4.6	A
Maximum Power Dissipation	$P_D$	$T_A=25^\circ C$	1.2	W
		$T_A=70^\circ C$	0.9	W
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	100	°C/W	

**MOSFET ELECTRICAL CHARACTERISTICS** Ta=25 °C unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	--	--	V
Zero Gate Voltage Drain Current(TA=25°C)	$I_{DSS}$	$V_{DS}=24V, V_{GS}=0V$	--	--	1	$\mu A$
Zero Gate Voltage Drain Current(TA=125°C)		$V_{DS}=24V, V_{GS}=0V$	--	--	100	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1.2	V
Drain-Source On-State Resistance②	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=5.8A$	--	27	35	m $\Omega$
Drain-Source On-State Resistance②	$R_{DS(ON)}$	$V_{GS}=3.3V, I_D=4A$	--	29	45	m $\Omega$
Drain-Source On-State Resistance②	$R_{DS(ON)}$	$V_{GS}=2.5V, I_D=2A$	--	35	50	m $\Omega$

**Dynamic Characteristics (note 4,5)**

Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	--	635	--	pF
Output Capacitance	$C_{oss}$		--	135	--	pF
Reverse Transfer Capacitance	$C_{rss}$		--	40	--	pF
Total Gate Charge	$Q_g$	$V_{DS}=15V, I_D=5A, V_{GS}=4.5V$	--	10.5	--	nC
Gate Source Charge	$Q_{gs}$		--	1.6	--	nC
Gate Drain Charge	$Q_{gd}$		--	2.7	--	nC

**Switching Characteristics (note 4,5)**

Turn on Delay Time	$t_{d(on)}$	$V_{DS}=15V, I_D=5A, R_G=3.3\Omega, V_{GS}=4.5V$	--	7.5	--	ns
Turn on Rise Time	$t_r$		--	18	--	ns
Turn Off Delay Time	$t_{d(off)}$		-	36	--	ns
Turn Off Fall Time	$t_f$		--	5	--	ns

**Drain-source diode characteristics and maximum ratings**

Source drain current(Body Diode)	$I_{SD}$	TA=25°C	--	--	1.5	A
Forward on voltage②	$V_{SD}$	Tj=25°C, ISD=3A, VGS=0V	--	0.82	1.2	V

**Notes:**

① Pulse width limited by maximum allowable junction temperature

② Pulse test ; Pulse width 300  $\mu s$ , duty cycle 2%.

RATINGS AND CHARACTERISTIC CURVES

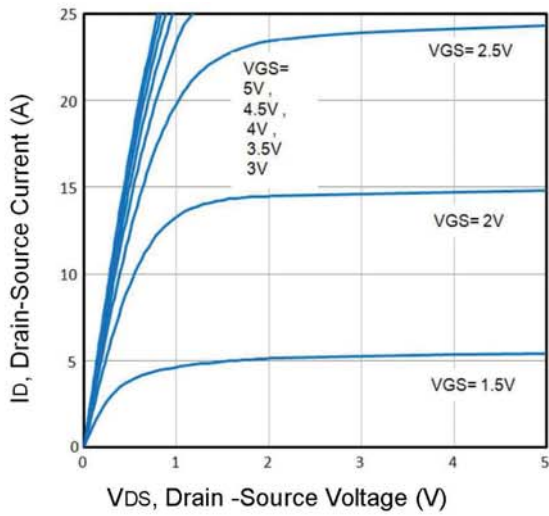


Fig1. Typical Output Characteristics

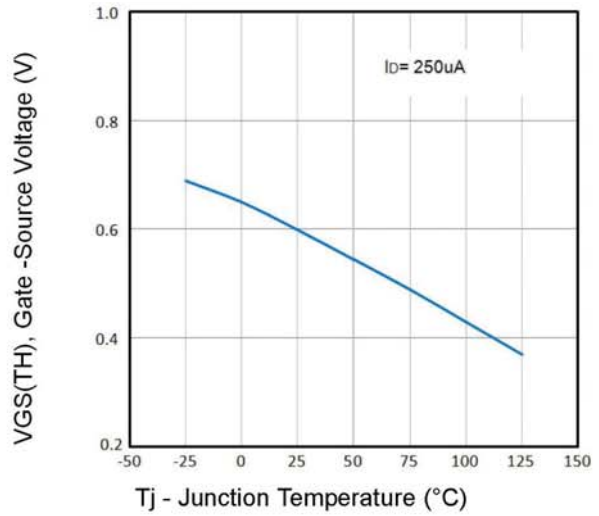


Fig2. Normalized Threshold Voltage Vs. Temperature

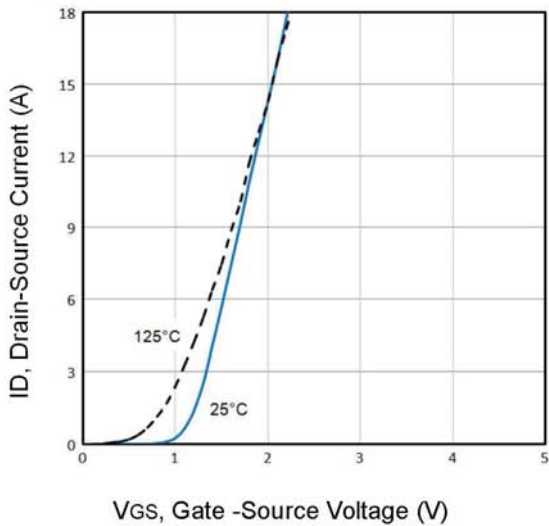


Fig3. Typical Transfer Characteristics

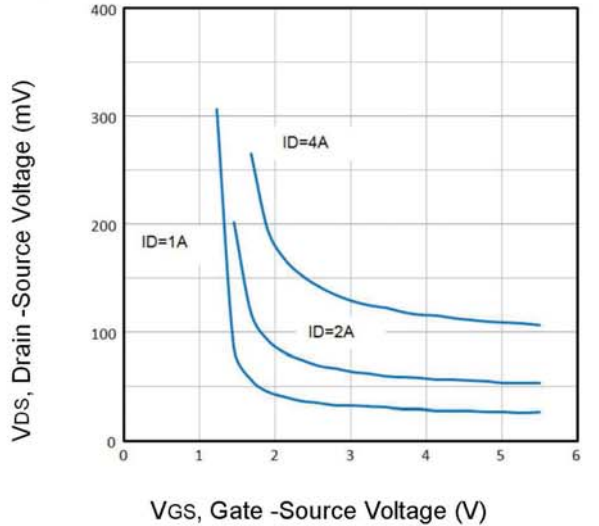


Fig4. Drain-Source Voltage vs Gate-Source Voltage

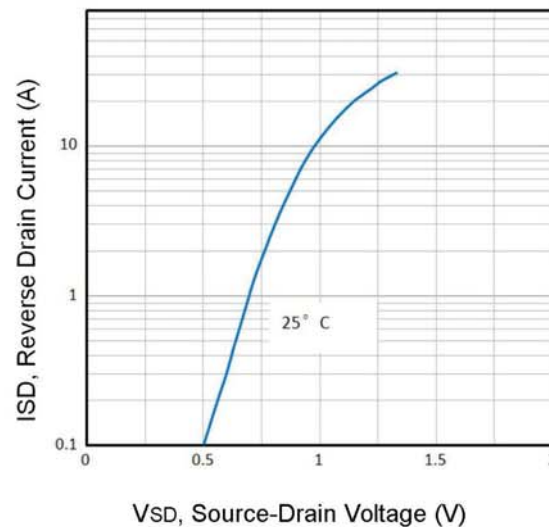


Fig5. Typical Source-Drain Diode Forward Voltage

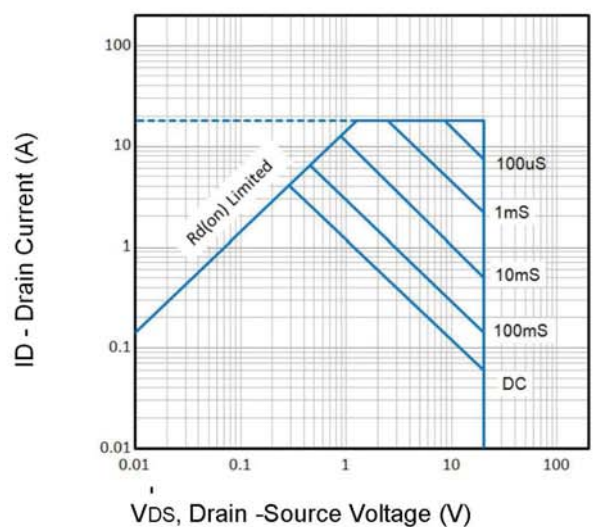


Fig6. Maximum Safe Operating Area

## RATINGS AND CHARACTERISTIC CURVES

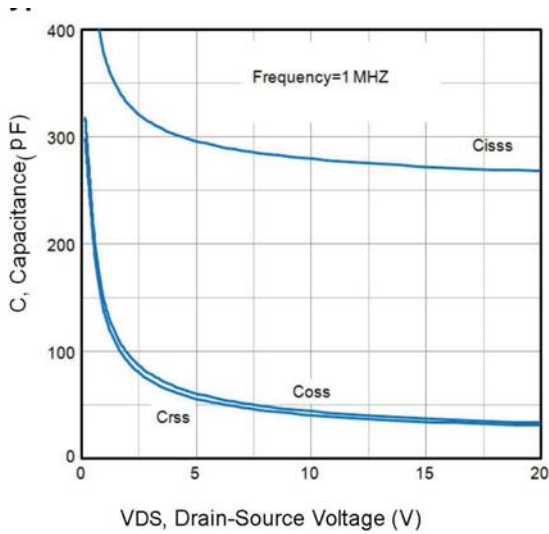


Fig7. Typical Capacitance Vs. Drain-Source Voltage

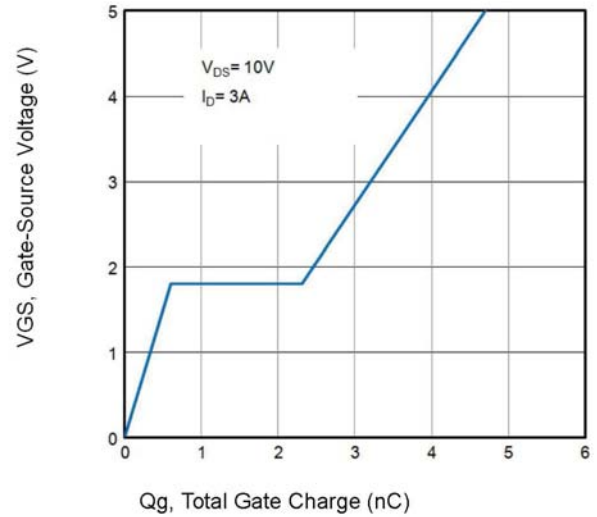


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

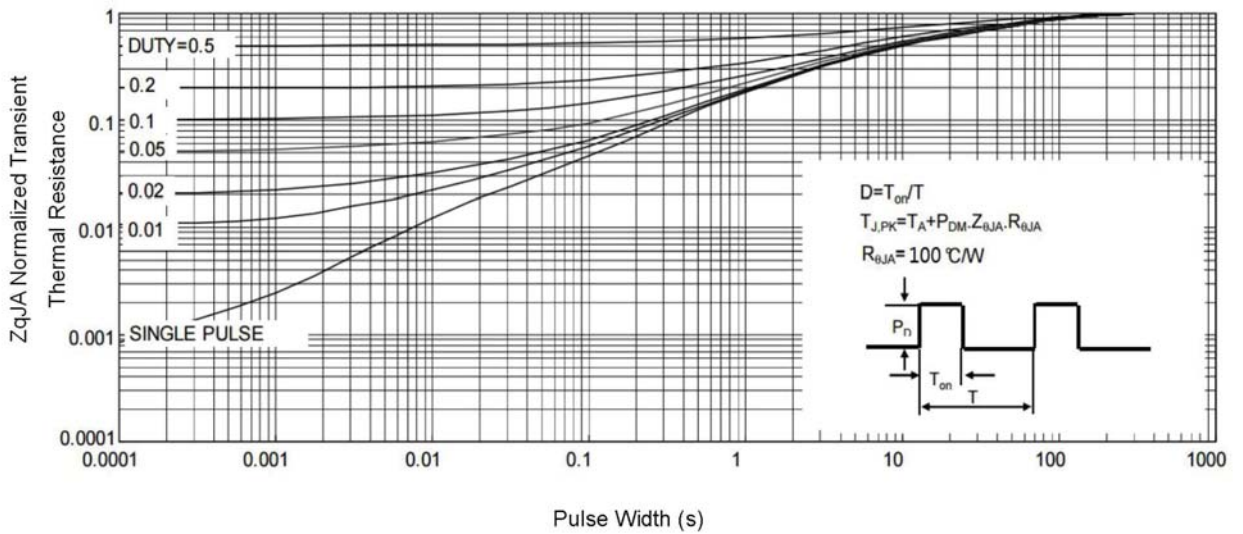


Fig9. Normalized Maximum Transient Thermal Impedance

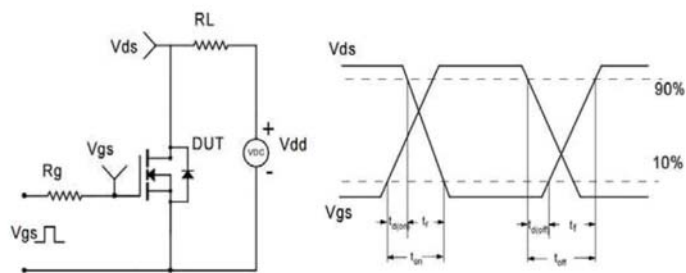


Fig10. Switching Time Test Circuit and waveform